PROCESS AND DEVICE FOR EVALUATING A CMOS LOGICAL CELL

Abstract of the Disclosure

The process includes modeling the cell and a phase for determining internal potentials of the cell based on operational simulation of the modeled cell utilizing a periodic binary stimulation signal. The floating substrate of each transistor of the cell, at predetermined successive instants of injection, is injected with a charge proportional to the variation of the internal potential of this transistor. A variation is determined during a predetermined time interval of the stimulation signal preceding the current instant of injection and exempt from injection, to accelerate the charge or the discharge of the floating substrate of the transistor.